ADAPTIVE CAPACITANCE FOR TRANSISTOR

BACKGROUND

Trench metal oxide semiconductor (MOS) transistors have been used as power transistors for switching external loads. Trench MOS transistors are one type of power transistor that exhibits electromagnetic susceptibility (EMS). EMS quantifies the immunity of a transistor switch to noise. If the transistor has a poor EMS, it may incorrectly switch from an off state to an on state in response to noise. This can be problematic in a noisy environment.

In one prior device, the power transistor had a gate switchably coupled through a resistor to a source. The gate and source were connected by the switch when it was desired to keep the power transistor in an off state. Since the gate and source were connected, the voltage between them was minimal, and the power transistor remained off. The switch was open when it was desired to allow the power transistor to be in an on state as controlled by a difference between the gate voltage and source voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic cross section of a transistor according to an example embodiment.

FIG. **2** is a circuit diagram of a transistor with an adaptive capacitance according to an example embodiment.

FIG. **3** is a block diagram of an alternative geometry for a MOS transistor according to an example embodiment.

FIG. **4** is a block diagram of a further alternative geometry for a MOS transistor according to an example embodiment.

FIG. **5** is a circuit diagram of a transistor with an adaptive capacitance and resistance according to an example embodiment.

FIG. **6** is a flowchart illustrating use of switches to selectively control coupling of a capacitor and resistor to a transistor according to an example embodiment.

DETAILED DESCRIPTION

In the following description, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration specific embodiments which may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that structural, logical and electrical changes may be made without departing from the scope of the present invention. The following description of example embodiments is, therefore, not to be taken in a limited sense, and the scope of the present invention is defined by the appended claims.

A trench MOS transistor with dynamic switchable capacitance provides improved electromagnetic susceptibility (EMS) for high frequency noise. In various embodiments, additional contacts to existing structures may be provided to obtain the switchable capacitance between a gate and source of the transistor. Several alternative geometries of power transistors are described, and an additional switch for providing a switchable resistance between the gate and source is provided such that both high and low frequency noise EMS may be improved.

FIG. **1** is a schematic cross section of an example trench MOS transistor indicated generally at **100**. In one embodiment, trench transistor **100** is a metal oxide semiconductor

(MOS) power transistor which may be formed in a conventional manner supported by a substrate. Additional circuitry may be formed on the same substrate. A drain **110** may be supported by the substrate or formed in the substrate as illustrated. An insulator filled trench **115** is formed, extending down into the drain **110**. Within the insulator filled trench **115**, a gate layer or structure **120** is formed, extending into the trench **115**. An additional electrode structure **125** is formed about a top of the gate and is separated from the gate structure by an insulated spacer.

The electrode structure **125** in one embodiment is integral with the gate structure. In one embodiment, the electrode structure **125** is formed within a chip area corresponding to the gate layer **125** and is proximate thereto. The electrode structure **125** originally is an affect left from an MOS process utilized in the manufacture of transistor **100** and facilitated planarization of the surface of transistor **100**. A bulk region **130** is formed above the drain and is insulated from the drain by an insulating region **135**. A source **140** is formed above the bulk region **130** and is also insulated from the bulk region **130** at **145**. A channel **150** is formed between a top portion of the gate **120** and the bulk region **130** and source **140**. The drain **110** may be further divided into a higher doped n type drain region that extends below the trench **115** along with a lower doped n-type drift region above the drain region. In one embodiment, the drain region may extend up as high as portions of the trench **115**.

In one embodiment, the gate structure **120** and electrode structure **125** comprise multiple levels, and may be formed of polysilicon. The levels form an integrated structure for the transistor **100**. Insulation spacers and areas may be formed of oxides in various embodiments. Similar semiconductor materials may be used in place of polysilicon, and other insulative materials may be used for the oxide.

Contacts are normally formed to the drain **110**, gate structure **120** and source **140**. A resistor may be selectively coupled by a switch between the gate and source contacts in one embodiment. This provides the ability to keep the transistor **100** in an off state when it is used to couple the gate and source. The resistance has usually been in the 1 kΩ to 2 kΩ range. The value of the resistor may be determined from ESD self protection requirements. For low frequency disturbances, the transistor **100** has a very high impedance at each terminal, and the resistor works as a good short circuit between the gate and source terminals.

For high frequency disturbances, the transistor **100** may have much lower impedance at the terminals, so the resistor cannot be a good short circuit. Dynamically, $V_{GS} \neq 0$ is allowed and this can drive the transistor into the on state, reducing EMS. In such high frequency ranges, the internal transistor **100** capacitances from gate to source and from gate to drain, play a significant role in defining the EMS. These capacitances drive the gate voltage working one against the other, as in a capacitive voltage divider. A gate to source capacitance, C_{GS} and gate to drain capacitance, C_{GD} are normally determined by the internal capacitances of a transistor.

Increasing C_{GS} at constant C_{GD} (increasing the C_{GS}/C_{GD} ratio) will result in a better EMS. To increase C_{GS}, additional on-chip capacitors with capacitances of the same order magnitude as the transistor's internal capacitances, if added, would consume additional chip area, increasing costs. Adding such additional capacitances external to the chip would result in an increase in the number of components, also increasing costs. Both of these alternatives are undesirable.

In one embodiment shown at **200** in FIG. **2**, an additional electrode terminal **210** is formed to the electrode structure **125**. In the circuit diagram of FIG. **2**, the transistor is indicated